REMARKS/ARGUMENTS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 281-286 are pending, wherein claims 281-286 are currently amended, and claims 1-280 are canceled.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 281

As currently amended, independent claim 281 is recited below:

281. A method for fabricating a circuitry component, comprising:

joining a die and a substrate, wherein said die has a top surface at a horizontal level; and

after said joining said die and said substrate, depositing a gold bump over said horizontal level.

Reconsideration of Claim 281 rejected under 35 U.S.C. 102(b) as being anticipated by Sakurai (US6,078,104) is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 281 patentably distinguishes over the citations by Sakurai (US6,078,104).

Sakurai teaches that a method for fabricating a circuitry component comprises depositing a copper bump 6 or 66 covered by gold plating over a horizontal level defined by a top surface of a die 1. ~ *See FIGS. 2 and 3, and col. 6, lines 33-44* ~ However, the bump 6 or 66 is a copper bump covered by gold plating taught by Sakurai, but not a gold bump as claimed in claim 281. The bump 6 or 66 taught by Sakurai comprises gold plating covering a copper body, but Sakurai fails to teach, hint or suggest the bump 6 or 66 is gold bump whose principal material is gold.

Applicants teach a method for fabricating a circuitry component comprises depositing a gold bump over a horizontal level defined by a top surface of a die, wherein the gold bump means that the principal material of the bump is gold, which is not taught by Sakurai. Applicants considers that claim 281 should be patentable because Sakurai fails to teach, hint or suggest the subject matter of depositing a gold bump whose principal material is gold over a horizontal level defined by a top surface of a die.

For at least the foregoing reasons, applicants respectfully submit independent claim 281 patently distinguishes over the prior art references, and should be allowed.

Response to Claim 282

As currently amended, independent claim 282 is recited below:

282. A method for fabricating a circuitry component, comprising:

joining multiple dies and a substrate;

depositing an insulating layer over said multiple dies and said substrate, wherein said insulating layer comprises a porous structure; and

separating said substrate into multiple portions.

Reconsideration of Claim 282 rejected under 35 U.S.C. 102(b) as being anticipated by Wojnarowski et al. (US5,576,517) is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 282 patentably distinguishes over the citation by Wojnarowski et al. (US5,576,517).

Wojnarowski et al. teach that a method for fabricating a circuitry component comprises joining a die 14 and a substrate 10 and depositing an insulating layer 20 over the die 14, wherein the insulating layer 20 comprises a porous structure. ~ *See FIGS. 1 and 2, and col. 5, lines 1-15* ~ However, Wojnarowski et al. fails to teach, hint or suggest the subject matters that multiple dies can be joined with the substrate 10 and that the substrate 10 can be separated into multiple portions, which are claimed in claim 282.

For at least the foregoing reasons, applicants respectfully submit independent claim 282 patently distinguishes over the prior art references, and should be allowed.

Response to Claim 283

As currently amended, independent claim 283 is recited below:

283. A method for fabricating a circuitry component, comprising:

joining multiple dies and a substrate, wherein one of said multiple dies has a top surface at a horizontal level; and

after said joining said multiple dies and said substrate, depositing a passive device over said horizontal level; and

separating said substrate into multiple portions.

Reconsideration of Claim 283 rejected under 35 U.S.C. 102(b) as being anticipated by Kunimatsu et al. (US5,767,564) is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 283 patentably distinguishes over the citation by Kunimatsu et al (US5,767,564).

Kunimatsu et al. teach that a method for fabricating a circuitry component comprises joining a die 2 and a substrate 1, and depositing a passive device 3 over a horizontal level defined by a top surface of the die 2. ~ *See FIG. 3, and col. 4, lines 22-37* ~ However, Kunimatsu et al. fail to teach, hint or suggest the subject matters that multiple dies can be joined with the substrate 1 and that the substrate 1 can be separated into multiple portions, which are claimed in claim 283.

For at least the foregoing reasons, applicants respectfully submit independent claim 283 patently distinguishes over the prior art references, and should be allowed.

Response to Claim 284

As currently amended, independent claim 284 is recited below:

284. A method for fabricating a circuitry component, comprising:

joining multiple dies and a substrate, wherein one of said multiple dies has a top surface at a horizontal level;

depositing a waveguide over said horizontal level; and

separating said substrate into multiple portions.

Reconsideration of Claim 284 rejected under 35 U.S.C. 102(e) as being anticipated by Yoshimura et al. (US6,690,845) is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 284 patentably distinguishes over the citation by Yoshimura et al. (US6,690,845).

Yoshimura et al. teach that a method for fabricating a circuitry component comprises joining multiple dies 904A and 904B and a substrate 412', and depositing a waveguide 1005 over a horizontal level defined by a top surface of one of the dies 904A and 904B. ~ *See FIGS. 170-176* ~ However, Yoshimura et al. fail to teach, hint or suggest the subject matter that the substrate 412' can be separated into multiple portions, which is claimed in claim 284.

For at least the foregoing reasons, applicants respectfully submit independent claim 284 patently distinguishes over the prior art references, and should be allowed.

Response to Claim 285

As currently amended, independent claim 285 is recited below:

285. A method for fabricating a circuitry component, comprising:
providing a die having a top surface at a horizontal level; and
depositing a micro electronic mechanical sensor (MEMS) over said horizontal level.

Reconsideration of Claim 285 rejected under 35 U.S.C. 103(a) as being unpatentable over Felton et al. (US6,759,273) is requested based on the following

remarks.

Applicants respectfully assert that the method claimed in claim 285 patentably distinguishes over the citation by Felton et al. (US6,759,273).

Felton et al. teach that a method for fabricating a circuitry component comprises depositing a micro electronic mechanical structure 5 over a wafer 1 before the wafer 1 is separated into multiple dies. ~*See FIG. 1*~

However, applicants teach a micro electronic mechanical sensor (MEMS) can be deposited over a horizontal level defined by a top surface of a die after being separated from a wafer, which is not taught by Felton et al.

"Die" is typically well-known as a body separated from "Wafer". The step of "depositing a micro electronic mechanical sensor (MEMS) over the horizontal level defined by a top surface of a die" claimed in Claim 285 means "depositing a micro electronic mechanical sensor (MEMS) over the horizontal level defined by a top surface of a die after being separated from a wafer". The step of "depositing a micro electronic mechanical sensor (MEMS) over a wafer" taught by Felton et al. means "depositing a micro electronic mechanical sensor (MEMS) over a wafer before being separated into multiple dies". Applicants consider that those skilled in the art should not come up with the subject matter claimed in claim 285 because Felton et al. fail to teach the step of depositing a micro electronic mechanical sensor (MEMS) over the horizontal level defined by a top surface of a die after being separated from a wafer, but teach the step of depositing a micro electronic mechanical sensor (MEMS) over a wafer before being separated into multiple dies.

The Examiner considers that "it would have been obvious to a person of ordinary

skill in the art at the time the invention was made modify the method of Felton et al. by dicing the wafer into plurality of dies and forming the MEMS individually, instead of forming in mass produce, since the process of making individual MEMS is simpler and within the ordinary designing ability expected of a person skilled in the art". ~ *See the last paragraph in page 4, in the last Office Action mailed on Mar. 1, 2006* ~ Applicants respectfully traverse the Examiner's opinions. Even instead of forming in mass produce, those skilled in the art should form MEMS devices over a wafer, based on the teachings by Felton et al., but should not come up with the concept that a MEMS device is deposited over a horizontal level defined by a top surface of a die after being separated from a wafer because Felton et al. fail to teach, hint or suggest the concept. If the Examiner considers the concept is possibly come up with by those skilled in the art at the time the invention was made modify the method of Felton et al., please show an evidence to support the Examiner's opinions.

For at least the foregoing reasons, applicants respectfully submit independent claim 285 patently distinguishes over the prior art references, and should be allowed.

Response to Claim 286

As currently amended, independent claim 286 is recited below:

286. A method for fabricating a circuitry component, comprising:
depositing an insulating layer over a circuitry element;
curing said insulating layer;
grinding said insulating layer; and
depositing a metal layer over said insulating layer.

Reconsideration of Claim 286 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger (US5,111,278) in view of Fasano et al. (US6,139,666) is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 286 patentably distinguishes over the citations by Eichelberger (US5,111,278) and by Fasano et al. (US6,139,666).

Eichelberger teaches that a method for fabricating a circuitry component comprises depositing an insulating layer 208 over a circuitry element 204, lapping the insulating layer 208, and depositing a metal layer 209 over the insulating layer 208. *~See FIG. 17, and col. 24, lines 3-6 ~* However, Eichelberger fails to teach, hint or suggest the subject matter of curing the insulating layer 208.

Applicants consider that claim 286 should be patentable because both Eichelberger and Fasano et al. fail to teach, hint or suggest that an insulating layer deposited over a circuitry element may be cured and ground.

For at least the foregoing reasons, applicants respectfully submit independent claim 286 patently distinguishes over the prior art references, and should be allowed.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 281-286 are in proper condition for allowance.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)